

**Digital Logic Lab Assignment \*7\***

* To verify the operation of Half Adder Circuit
* To verify the operation of Full Adder Circuit
* To construct a Full Adder Circuit using 2 Half Adders

**Submitted By**

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Year I / SEM I

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**OBJECTIVE 7.1:**

**TO VERIFY THE OPERATION OF HALF ADDER CIRCUIT.**

**THEORY:**

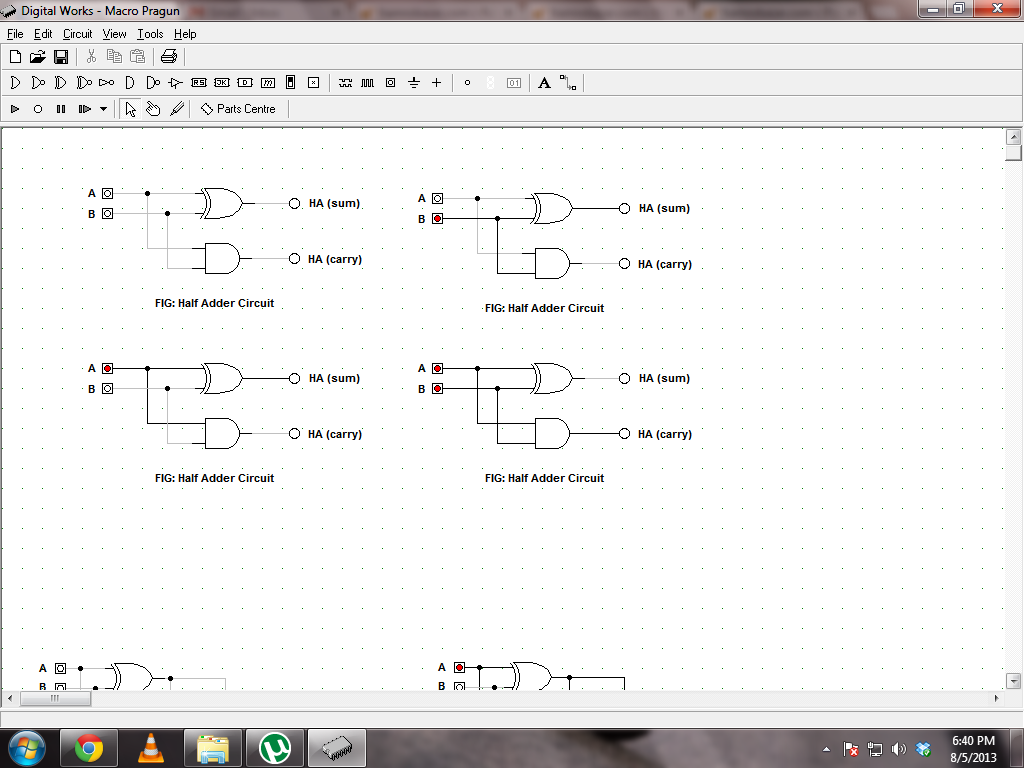
The half adder is an example of a simple, functional digital circuit built from two logic gates.  The half adder adds two one-bit binary numbers (AB).  The output is the sum of the two bits (S) and the carry (C).

**Boolean Expressions:**

Sum = A’B+AB’ = A⊕B

Carry = AB

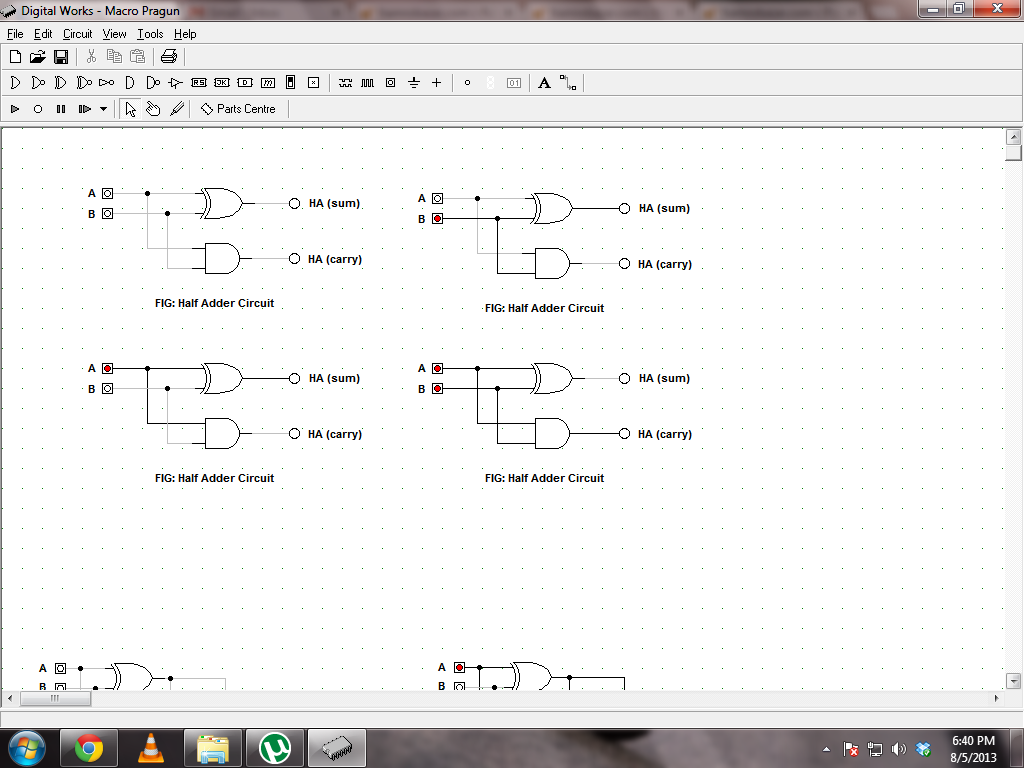
**CIRCUIT DIAGRAM:**



**TRUTH TABLE:**

|  |  |  |  |
| --- | --- | --- | --- |
| **A** | **B** | **Carry** | **Sum** |
| 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 |

**OBSERVATIONS:**



**OBSERVATION TABLE:**

|  |  |  |  |
| --- | --- | --- | --- |
| **A** | **B** | **Carry** | **Sum** |
| 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 |

**CONCLUSION:**

Hence, operation of Half Adder is verified.

**REFERENCE:**

<http://isweb.redwoods.edu/instruct/calderwoodd/diglogic/half-add.htm>

**OBJECTIVE 7.2:**

**TO VERIFY THE OPERATION OF FULL ADDER CIRCUIT.**

**THEORY:**

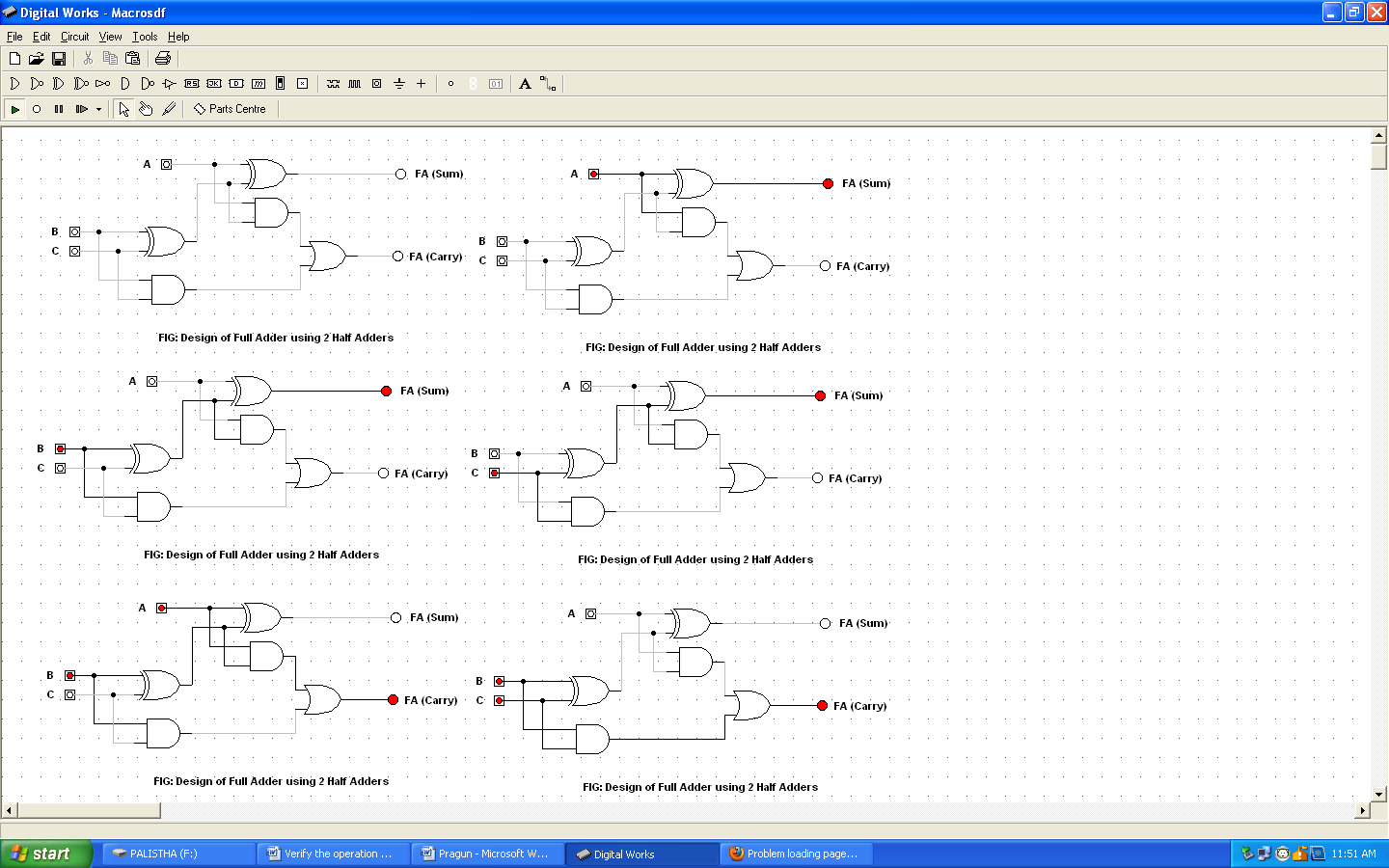
The full-adder circuit adds three one-bit binary numbers (C A B) and outputs two one-bit binary numbers, a sum (S) and a carry (C1).   The full-adder is usually a component in a cascade of adders, which add 8, 16, 32, etc. binary numbers.  The carry input for the full-adder circuit is from the carry output from the circuit "above" itself in the cascade.  The carry output from the full adder is fed to another full adder "below" itself in the cascade.

**Boolean Expressions:**

Sum = A’B’C+A’BC’+AB’C’+ABC = C(A⊕B)+AB

Carry = C⊕(A⊕B) = A’BC+AB’C+ABC’+ABC

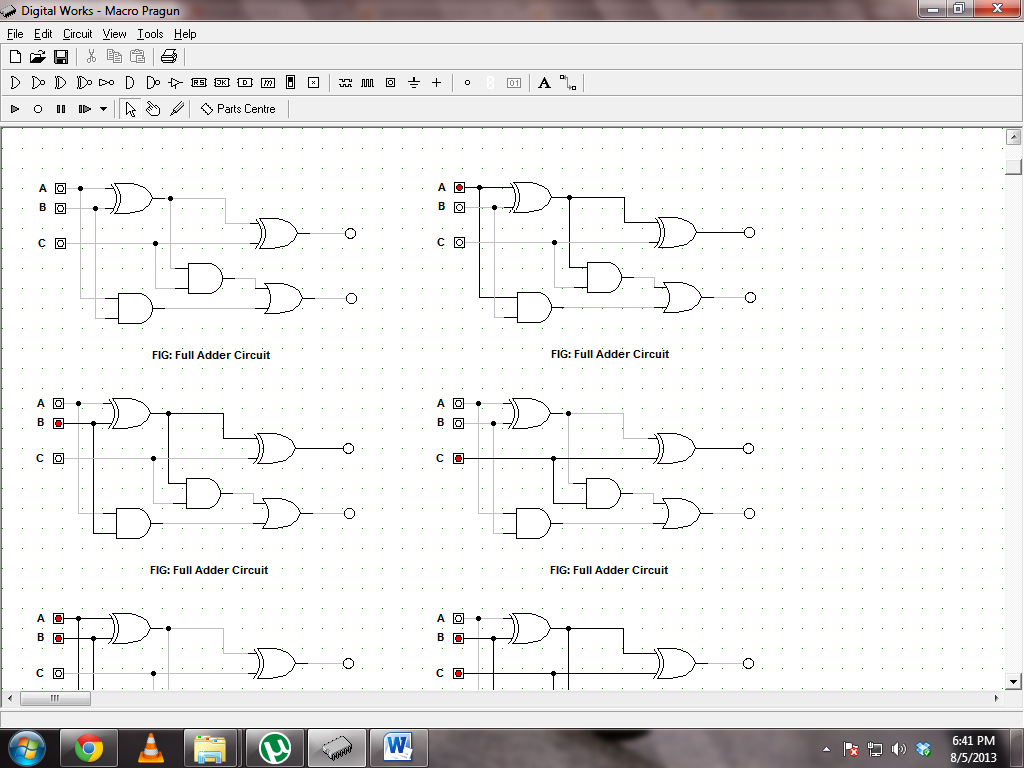
**CIRCUIT DIAGRAM:**

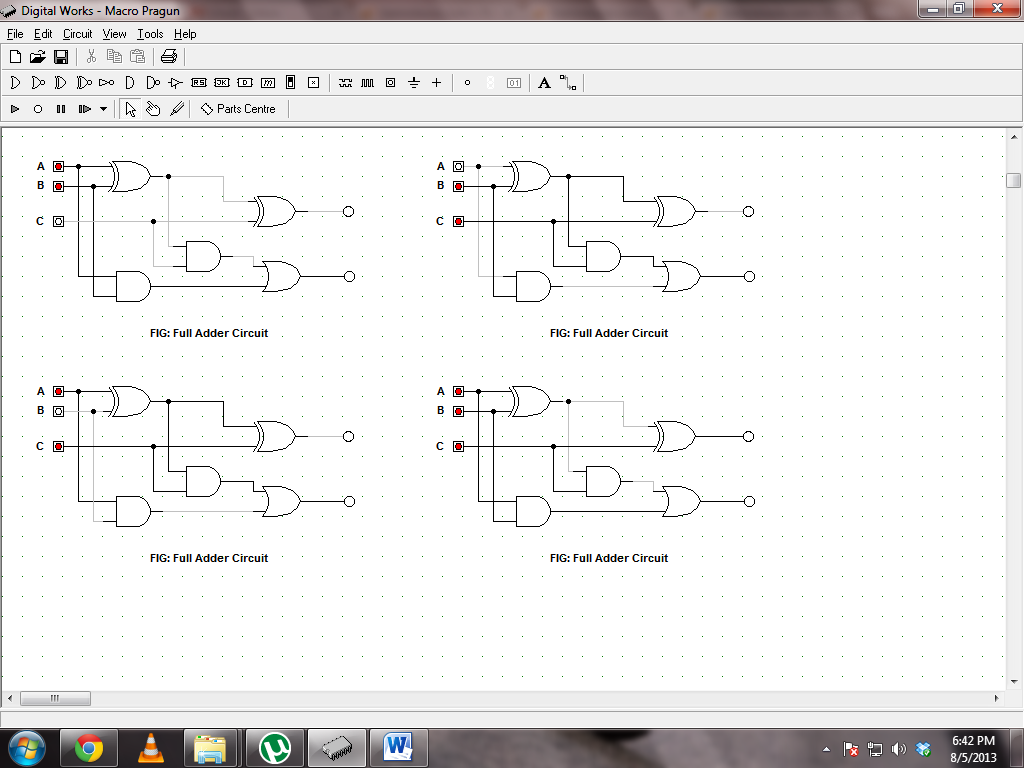


**TRUTH TABLE:**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **A** | **B** | **C** | **Carry** | **Sum** |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 |
| 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 1 | 1 |

**OBSERVATIONS:**





**OBSERVATION TABLE:**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **A** | **B** | **C** | **Carry** | **Sum** |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 |
| 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 1 | 1 |

**CONCLUSION:**

Hence, operation of Full Adder is verified.

**REFERENCE:**

<http://isweb.redwoods.edu/instruct/calderwoodd/diglogic/half-add.htm>

**OBJECTIVE 7.3:**

**TO CONSTRUCT FULL ADDER USING 2 HALF ADDERS.**

**THEORY:**

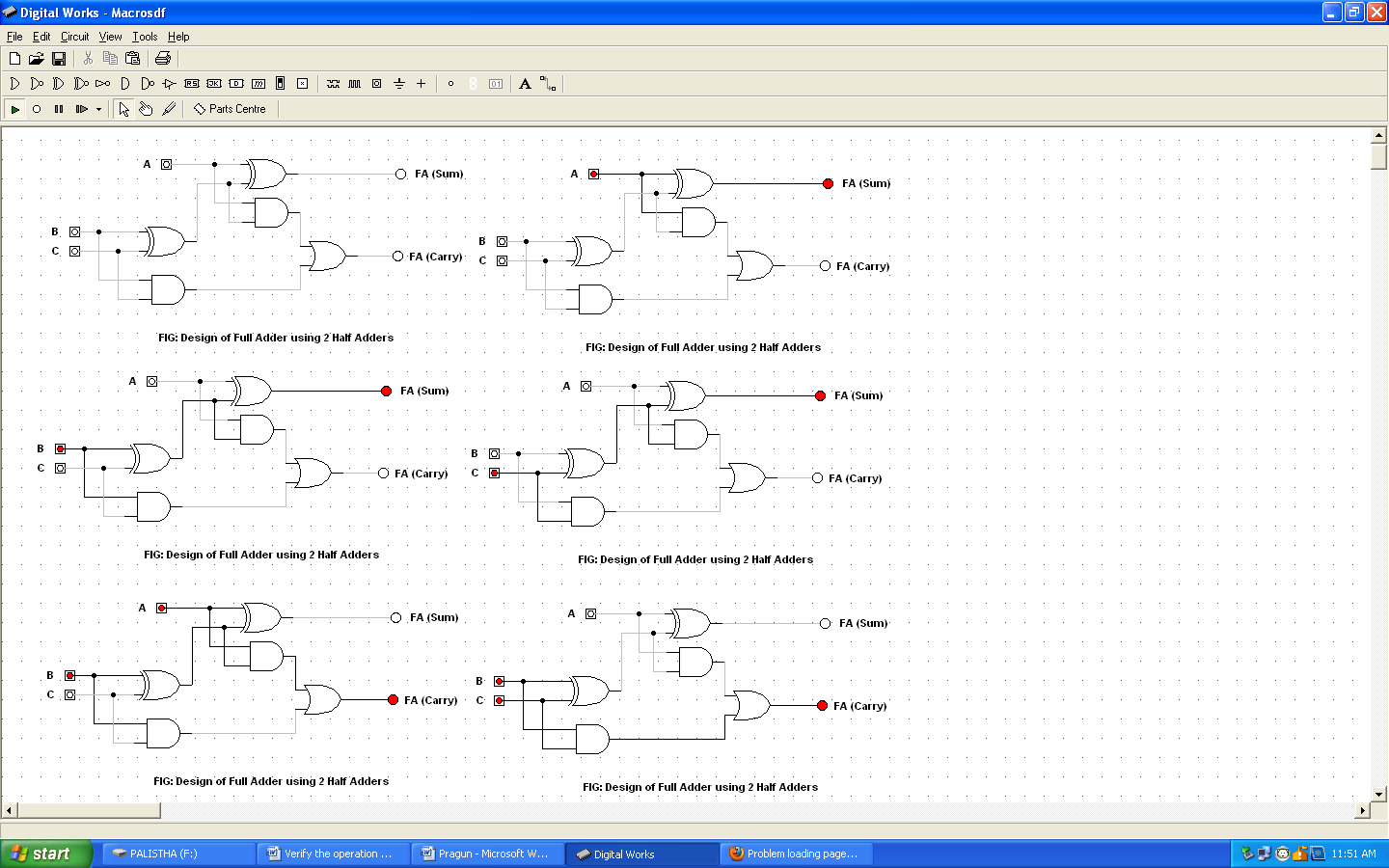
The full-adder circuit adds three one-bit binary numbers (C A B) and outputs two one-bit binary numbers, a sum (S) and a carry (C1).   The full-adder is usually a component in a cascade of adders, which add 8, 16, 32, etc. binary numbers.  The carry input for the full-adder circuit is from the carry output from the circuit "above" itself in the cascade.  The carry output from the full adder is fed to another full adder "below" itself in the cascade.

**Boolean Expressions:**

Sum = A’B’C+A’BC’+AB’C’+ABC = C(A⊕B)+AB

Carry = C⊕(A⊕B) = A’BC+AB’C+ABC’+ABC

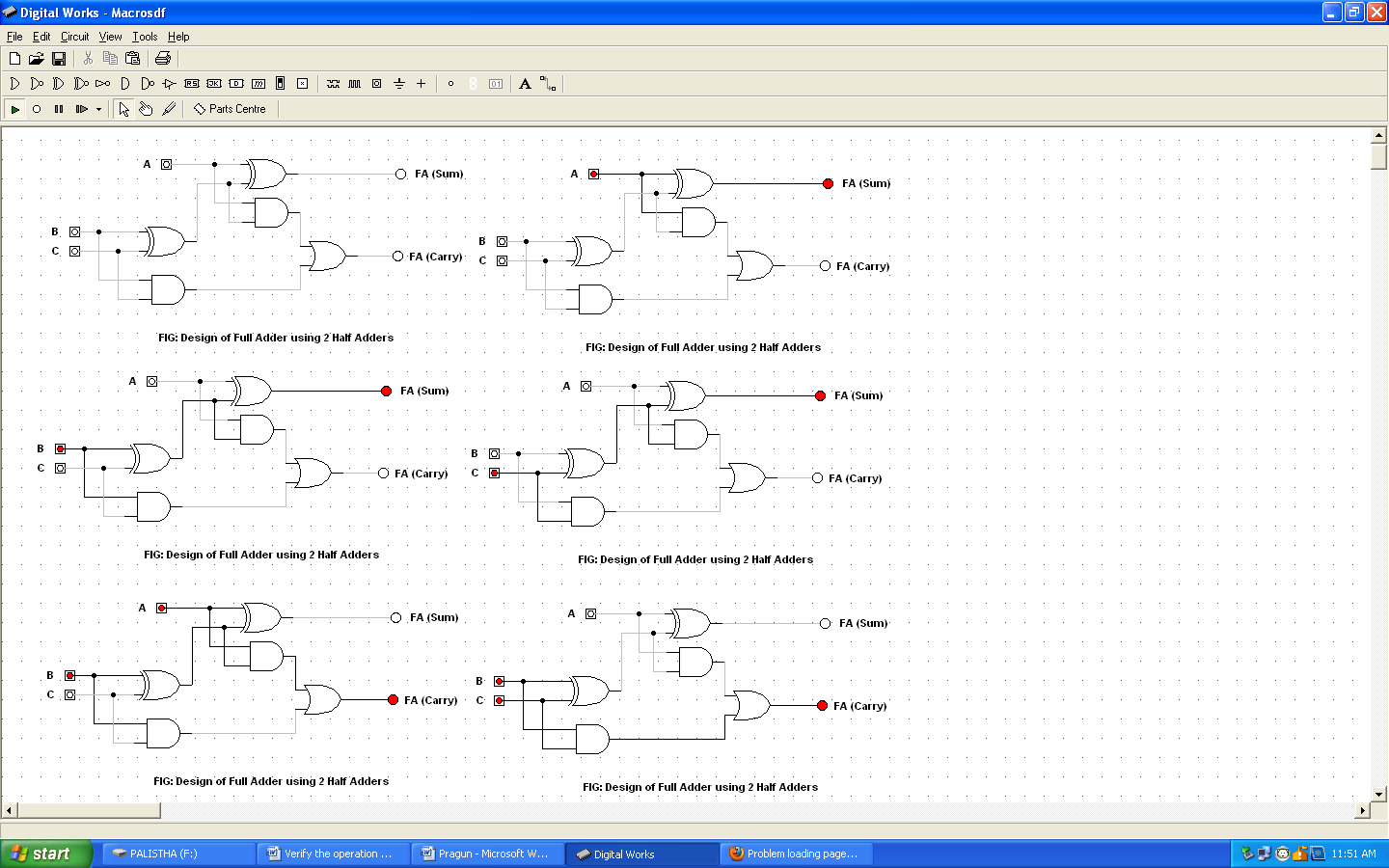
**CIRCUIT DIAGRAM:**

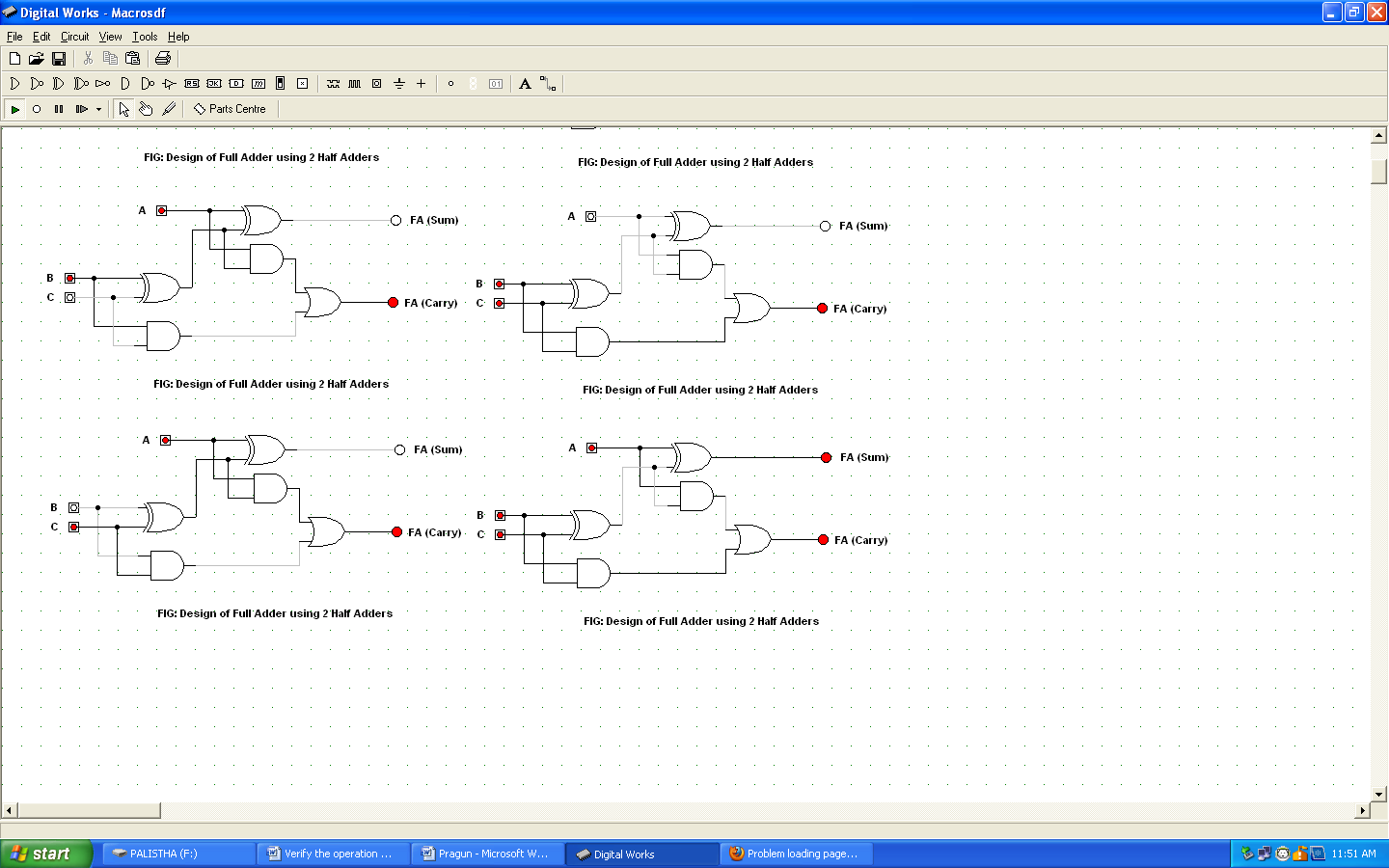


**TRUTH TABLE:**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **A** | **B** | **C** | **Carry** | **Sum** |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 |
| 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 1 | 1 |

**OBSERVATIONS:**





**OBSERVATION TABLE:**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **A** | **B** | **C** | **Carry** | **Sum** |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 |
| 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 1 | 1 |

**CONCLUSION:**

Hence, the full adder circuit was verified using 2 half adder circuits.

**REFERENCE:**

<http://isweb.redwoods.edu/instruct/calderwoodd/diglogic/half-add.htm>